REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1-53 are pending in the application. Claims 1-53 have been rejected. Claims 2 – 6, 26, 27, 36 – 38, 40 and 41 have been amended. Claims 1, 7 – 25, 28 – 35, 39, 42 – 53 have been cancelled without prejudice or disclaimer. Applicants reserve the right to file claims with the subject matter of these cancelled claims in continuation applications. Claims 54 – 63 have been added.

Applicants respectfully assert that the amendments to the claims add no new matter.

Claim Rejections

35 U.S.C. §102 Rejections

In the Office Action, the Examiner rejected claims 1 – 4, 7 – 9, 12 – 15, 17 – 22, 24 – 33, 36 – 44, 48, 50, 52 and 53 under 35 U.S.C. §102(e), as being anticipated by Elabd (US Patent 6,526,462).

Claims 1, 7 – 9, 12 – 15, 17 – 22, 24 – 25, 28 – 33, 39, 42 – 44, 48, 50, 52 and 53 have been cancelled without prejudice or disclaimer, thus rendering the rejection of these claims moot.

Applicants respectfully traverse the rejection of claims 2 – 4, 26 – 27, 36 – 38, and 40 – 41, in view of the remarks that follow.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. (MPEP 2131)

With regard to claims 2, 36 and 56, the Examiner referred to col 1, lines 60-66; Fig. 2, items 4, 30 and 34; col. 5, lines 39-50; col. 6, lines 24-67 to col. 7, lines 1-29; Fig. 5B, items M1-M6 and MEM1-MEM6; and generally Figs. 2, 5B and 10, and the accompanying text of Elabd.

Elabd does not anticipate claim 2, as amended, for at least the following reasons:

a) Claim 2 as amended recites: "at least two processing units with separate memories and separate busses."

The Examiner referred to column 1, lines 60 – 66, which describes Fig. 1. Fig. 1 shows at least two processing units of which processors 2 and 4 reside on bus 24, and processors 18, 20, and 22 reside on bus 28. Fig. 1 shows two memories: a cache memory included in processor 4, and internal/external memory 16, both of which share bus 24. Therefore, Fig. 1 and column 1, lines 60 – 66, fail to show "at least two processing units with separate memories and separate busses."

The Examiner referred to Fig. 2, item 4. Fig. 2 shows at least two processing units 2, 4, 18, 20, and 22, of which referenced item 4 is a CPU with cache memory. The only other memories shown in Fig. 2 are items 32 and 34, which do not share a bus with any of the aforementioned processing units, and which are shared resources, as indicated in column 5, line 67 to column 6, line 2: "The memory types that are accessible using the MT MMS 30 include SRAM FIFO memory 32 or internal/external memory 34..." Therefore, Fig. 2 fails to show "at least two processing units with separate memories and separate busses."

The Examiner referred to Fig. 5B, items M1 – M6 and MEM1 – MEM6. Column 10, lines 59 – 65 states: "Fig. 5B illustrates another example of an arbitration load balancing scheme... This example assumes that there are six masters M1, M2, M3, M4, M5, and M6; four buses BUS1, BUS2, BUS3, and BUS4 (memory threads or inter connections); and six memory banks MEM1, MEM2, MEM3, MEM4, MEM5, and MEM6." This shows that the memory banks shown in Fig. 5B are shared resources, which do not share a bus with any of

the masters. Therefore, Fig. 5B fails to show "at least two processing units with separate memories and separate busses".

The Examiner referred to column 6, lines 24 – 67 to column 7, lines 1 – 29. Column 6, lines 33 – 35, states: "...the MT MMS 30 includes a RCPU that manages the memory requests by routing/switching them between the masters", indicating that the memories do not share a bus with any specific processor, and failing to show "at least two processing units with separate memories and separate busses." Column 6, lines 43 – 61, describes Fig. 3, which is a variation of Fig. 2. The hereinabove comments relating to Fig. 2 apply equally to Fig. 3, which includes the same shared memories 32 and 34 that do not share a bus with any of processors 4, 18, 20, 22, 38 and 40. Therefore, Fig. 3 and column 6, lines 43 – 60, fail to show "at least two processing units with separate memories and separate busses." Column 6, lines 61 – 67, to column 7, lines 1 – 29, more particularly describe the operation of MT MMS 30, with reference to Fig. 4. As stated in column 5, line 67 to column 6, line 2: "The memory types that are accessible using the MT MMS 30 include SRAM FIFO memory 32 or internal/external memory 34..." The precise method of operation of MT MMS 30 is moot since access to shared memories 32 and 34 is inconsistent with "at least two processing units with separate memories and separate busses."

The Examiner referred to Fig. 10 and the accompanying text. Column 13, lines 47 – 50, states: "The microcontroller 180, memory 190A and peripherals 190B are connected to the 8 or 32 bit bus 210, as are the control status registers 170 of the various peripheral cores, a DSP 172, and the MT MMS 30B via a bridge 212." Thus, processors 172 and 180 are not shown to possess separate memories and separate busses. Fig. 10 shows that peripheral bus 330 is shared between multiple processors, none of which is shown to possess a separate memory. Therefore, Fig. 10 fails to show "at least two processing units with separate memories and separate busses."

b) Claim 2 as amended recites: "at least one first in first out (FIFO) unit to transfer said data between said busses; at least one first direct memory access (DMA) channel to transfer said data from one of said memories to said at least one FIFO unit; and at least one second DMA channel to transfer said data from said at least one FIFO unit to another of said memories."

The Examiner referred to column 1, lines 60 – 66, which describes Fig. 1. Fig. 1 and column 1, lines 60 – 66 do not show "at least one first in first out (FIFO) unit to transfer said data between said busses; at least one first direct memory access (DMA) channel to transfer said data from one of said memories to said at least one FIFO unit; and at least one second DMA channel to transfer said data from said at least one FIFO unit to another of said memories."

The Examiner referred to Fig. 2, item 32, which is a FIFO unit. Fig. 2 shows that item 32 does not share a bus with any of the processing units 2, 4, 18, 20, and 22, and that it is a shared resource, as indicated in column 5, line 67 to column 6, line 2: "The memory types that are accessible using the MT MMS 30 include SRAM FIFO memory 32 or internal/external memory 34..." Furthermore, column 2, lines 15 – 20 states "The DMA 6 is a direct memory access device that allows a peripheral device (master) to access the internal/external memory 16 without requiring the assistance of the processor (i.e., CPU 4) on the system bus 24. The DMA 6 will generally use an internal 32 bit FIFO for temporary storage of the DMA data." Therefore, Fig. 2 fails to show "at least one first in first out (FIFO) unit to transfer said data between said busses; at least one first direct memory access (DMA) channel to transfer said data from one of said memories to said at least one FIFO unit; and at least one second DMA channel to transfer said data from said at least one FIFO unit to another of said memories."

Elabd does not anticipate claim 36, as amended, for at least the following reasons:

a) Claim 36 as amended recites "a first memory directly accessible only by said first processing unit" and "a second memory directly accessible only by said second processing unit."

The Examiner referred to column 1, lines 60 – 66, which describes Fig. 1. Fig. 1 shows at least two processing units of which processors 2 and 4 reside on bus 24, and processors 18, 20, and 22 reside on bus 28. Fig. 1 shows two memories: a cache memory included in processor 4, and internal/external memory 16, both of which share bus 24. Therefore, Fig. 1 and column 1, lines 60 – 66, fail to show "a first memory directly accessible

only by said first processing unit" and "a second memory directly accessible only by said second processing unit".

The Examiner referred to Fig. 2, item 4. Fig. 2 shows at least two processing units 2, 4, 18, 20, and 22, of which referenced item 4 is a CPU with cache memory. The only other memories shown in Fig. 2 are items 32 and 34, which do not share a bus with any of the aforementioned processing units, and are shared resources, as indicated in column 5, line 67 to column 6, line 2: "The memory types that are accessible using the MT MMS 30 include SRAM FIFO memory 32 or internal/external memory 34..." Therefore, Fig. 2 fails to show "a first memory directly accessible only by said first processing unit" and "a second memory directly accessible only by said second processing unit."

The Examiner referred to Fig. 5B, items M1 – M6 and MEM1 – MEM6. Column 10, lines 59 – 65 states: "Fig. 5B illustrates another example of an arbitration load balancing scheme... This example assumes that there are six masters M1, M2, M3, M4, M5, and M6; four buses BUS1, BUS2, BUS3, and BUS4 (memory threads or inter connections); and six memory banks MEM1, MEM2, MEM3, MEM4, MEM5, and MEM6." This shows that the memory banks shown in Fig. 5B are shared resources, which do not share a bus with any of the masters. Therefore, Fig. 5B fails to show "a first memory directly accessible only by said first processing unit" and "a second memory directly accessible only by said second processing unit".

The Examiner referred to column 6, lines 24 – 67 to column 7, lines 1 – 29. Column 6, lines 33 – 35, states: "...the MT MMS 30 includes a RCPU that manages the memory requests by routing/switching them between the masters", indicating that the memories do not share a bus with any specific processor, and failing to show "a first memory directly accessible only by said first processing unit" and "a second memory directly accessible only by said second processing unit." Column 6, lines 43 – 61, describes Fig. 3, which is a variation of Fig. 2. The hereinabove comments relating to Fig. 2 apply equally to Fig. 3, which includes the same shared memories 32 and 34 that do not share a bus with any of processors 4, 18, 20, 22, 38 and 40. Therefore, Fig. 3 and column 6, lines 43 – 60, fail to show "a first memory directly accessible only by said first processing unit" and "a second memory directly accessible only by said second processing unit." Column 6, lines 61 – 67, to

column 7, lines 1 – 29, more particularly describe the operation of MT MMS 30, with reference to Fig. 4. As stated in column 5, line 67 to column 6, line 2: "The memory types that are accessible using the MT MMS 30 include SRAM FIFO memory 32 or internal/external memory 34..." The precise method of operation of MT MMS 30 is moot since access to shared memories 32 and 34 is inconsistent with "a first memory directly accessible only by said first processing unit" and "a second memory directly accessible only by said second processing unit."

The Examiner referred to Fig. 10 and the accompanying text. Column 13, lines 47 – 50, states: "The microcontroller 180, memory 190A and peripherals 190B are connected to the 8 or 32 bit bus 210, as are the control status registers 170 of the various peripheral cores, a DSP 172, and the MT MMS 30B via a bridge 212." Thus, processors 172 and 180 are not shown to possess separate memories and separate busses. Fig. 10 shows that peripheral bus 330 is shared between multiple processors, none of which is shown to possess a separate memory. Therefore, Fig. 10 fails to show "a first memory directly accessible only by said first processing unit" and "a second memory directly accessible only by said second processing unit".

b) Claim 36, as amended, recites "a first direct memory access (DMA) channel to a first in first out (FIFO) unit from a first memory" and "a second DMA channel to a FIFO unit from a second memory."

The Examiner referred to column 1, lines 60 – 66, which describes Fig. 1. Fig. 1 and column 1, lines 60 – 66, fail to show a "a first direct memory access (DMA) channel to a first in first out (FIFO) unit from a first memory" and "a second DMA channel to a FIFO unit from a second memory".

The Examiner referred to Fig. 2, item 32, which is a FIFO unit. Fig. 2 shows that item 32 does not share a bus with any of the processing units 2, 4, 18, 20, and 22, and that it is a shared resource, as indicated in column 5, line 67 to column 6, line 2: "The memory types that are accessible using the MT MMS 30 include SRAM FIFO memory 32 or internal/external memory 34..." Furthermore, column 2, lines 15 – 20 states "The DMA 6 is a direct memory access device that allows a peripheral device (master) to access the

internal/external memory 16 without requiring the assistance of the processor (i.e., CPU 4) on the system bus 24. The DMA 6 will generally use an internal 32 bit FIFO for temporary storage of the DMA data." Therefore, Fig. 2 fails to show "a first direct memory access (DMA) channel to a first in first out (FIFO) unit from a first memory" and "a second DMA channel to a FIFO unit from a second memory."

As demonstrated above, Elabd does not teach, either explicitly or implicitly, any of the above-quoted limitations of claims 2 and 36, and therefore Elabd cannot anticipate claims 2 and 36.

Claims 3 – 6, 26 and 27 are dependent, directly or indirectly, from claim 2, and include all of the limitations of the independent claim. Therefore, Elabd cannot anticipate claims 3 – 6, 26 and 27.

Claims 37, 38, 40 and 41 are dependent, directly or indirectly, from claim 36, and include all of the limitations of the independent claim. Therefore, Elabd cannot anticipate claims 37, 38, 40 and 41.

In view of the preceding remarks, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 2 – 4, 26 – 27, 36 – 38, and 40 – 41.

35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claims 1, 4, 7, 9, 12, 13, 42, 44, 45, 48, 49, 52 and 53 under 35 U.S.C. §103(a), as being unpatentable over Shih (US Patent 5,590,308) in view of Elabd.

In the Office Action, the Examiner rejected claims 1, 2, 4, 5, 7, 8, 10, 28, 30, 35, 42, 43 and 47 under 35 U.S.C. §103(a), as being unpatentable over Horst (US Patent 5,317,726) in view of Elabd.

In the Office Action, the Examiner rejected claims 6, 11, 16, 46, and 51 under 35 U.S.C. §103(a), as being unpatentable over Shih as applied to claims 1, 7, 12, 42, and 48 in view of Elabd, and further in view of US Patent Application Publication No. 2003/0009629 to Gruner.

In the Office Action, the Examiner rejected claim 23 under 35 U.S.C. §103(a), as being unpatentable over Elabd in view of Gruner.

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (MPEP 2143.03)

Shih fails to cure the deficiencies of Elabd. In particular, Shih does not teach or suggest the above-quoted limitations of amended claims 2 and 36, and new claim 56. Therefore, the Examiner's proposed modification of Elabd in view of the teachings of Shih is still missing at least one limitation of claims 2 and 36, as amended, and of new claim 56.

Horst fails to cure the deficiencies of Elabd. In particular, Horst does not teach or suggest the above-quoted limitations of amended claims 2 and 36, and new claim 56. Therefore, the Examiner's proposed modification of Elabd in view of the teachings of Horst is still missing at least one limitation of claims 2 and 36, as amended, and of new claim 56.

Gruner fails to cure the deficiencies of Elabd. In particular, Gruner does not teach or suggest the above-quoted limitations of amended claims 2 and 36, and new claim 56. Therefore, the Examiner's proposed modification of Elabd in view of the teachings of Gruner is still missing at least one limitation of claims 2 and 36, as amended, and of new claim 56.

In view of the preceding remarks, Applicants respectfully request that the rejection of claims 2, 4, 5 and 6 under 35 U.S.C. §103(a) be withdrawn.

Remarks to cited references

37 CFR 1.111(c) requires an Applicant to clearly point out the patentable novelty which Applicant thinks the newly added claims present in view of the state of the art disclosed by the references cited. According to MPEP 714.02 and 714.04, Applicant is to clearly point out the patentable novelty of a newly added claim by specifically pointing out how the language of the claim patentably distinguishes the claim from the references cited, in order to provide a complete prosecution record as to why the claim should be allowed over the prior art of record. Applicant has presented such arguments below for the new independent claim 56.

New claim 54 is dependent from claim 2 and new claim 55 is dependent from claim 36. Arguments have been given above regarding the allowability of amended claims 2 and 36.

New claim 56 recites a device comprising a chip. In particular, the chip includes "at least two processing units with separate memories and separate busses" and "at least one first in first out (FIFO) unit to transfer said data between said busses; and at least one first direct memory access (DMA) channel to transfer said data from one of said memories to said at least one FIFO unit; and at least one second DMA channel to transfer said data from said at least one FIFO unit to another of said memories." None of these limitations is taught or suggested in any of the references cited by the Examiner.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 05-0649.

Respectfully submitted,

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